Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.120”**



**.110”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004” min.**

**Backside Potential: COLLECTOR**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .110” X .120” DATE: 2/11/19**

**MFG: MOTOROLA THICKNESS .013” P/N: MJEC15030**

**DG 10.1.2**

#### Rev B, 7/1